Application Note

AWB20060413

Create a recipe to
detect repeater defects within layers

FEATURES

- Layer Repeater
- Process Options
- Distribution Repeater Map
- HTML Output
- Send via email

Siglaz

Introduction

This application note discusses a technique to improve the baseline yield using the *Layer Repeater* function in IDA. Defect excursions within the repeating layers, see Figure 1, may cause a loss in CP (chip probing) yield, and any delays in detecting the excursion may affect many work-in-progress wafers. Defect excursions of this type escape traditional detection method used in SPC, since the defect counts are typically well below the control limit.

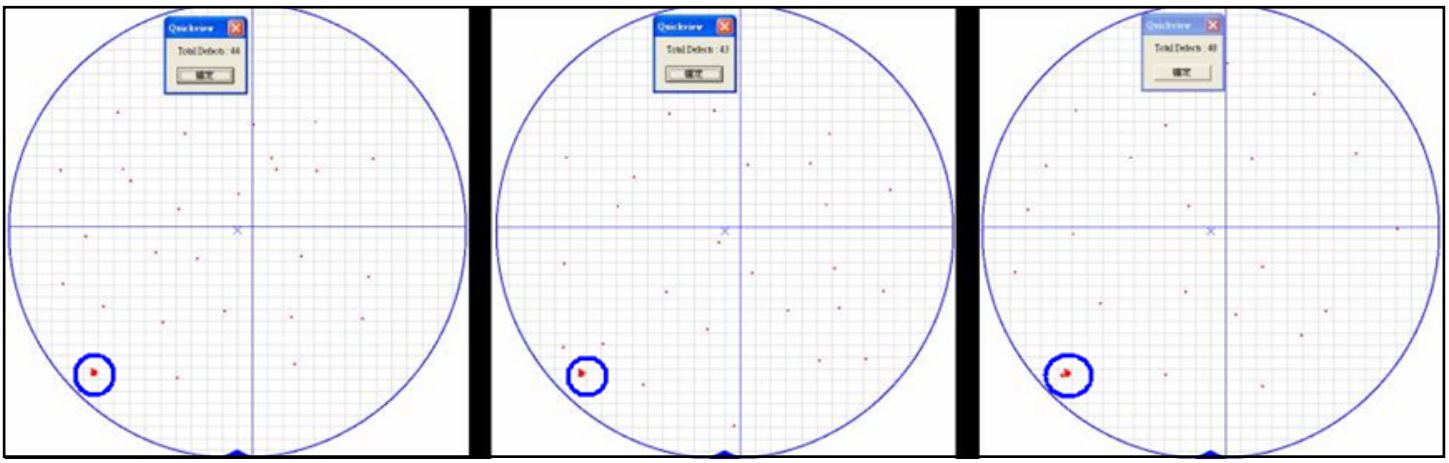

Figure 1 Layer repeaters

Layer repeaters are defects that occur systematically during the fabrication process, at a certain location in the surface of the wafer; they will escape detection unless a stack of wafer maps are overlaid using layer repeater analysis. Figure 2 illustrates the layer repeater concept.

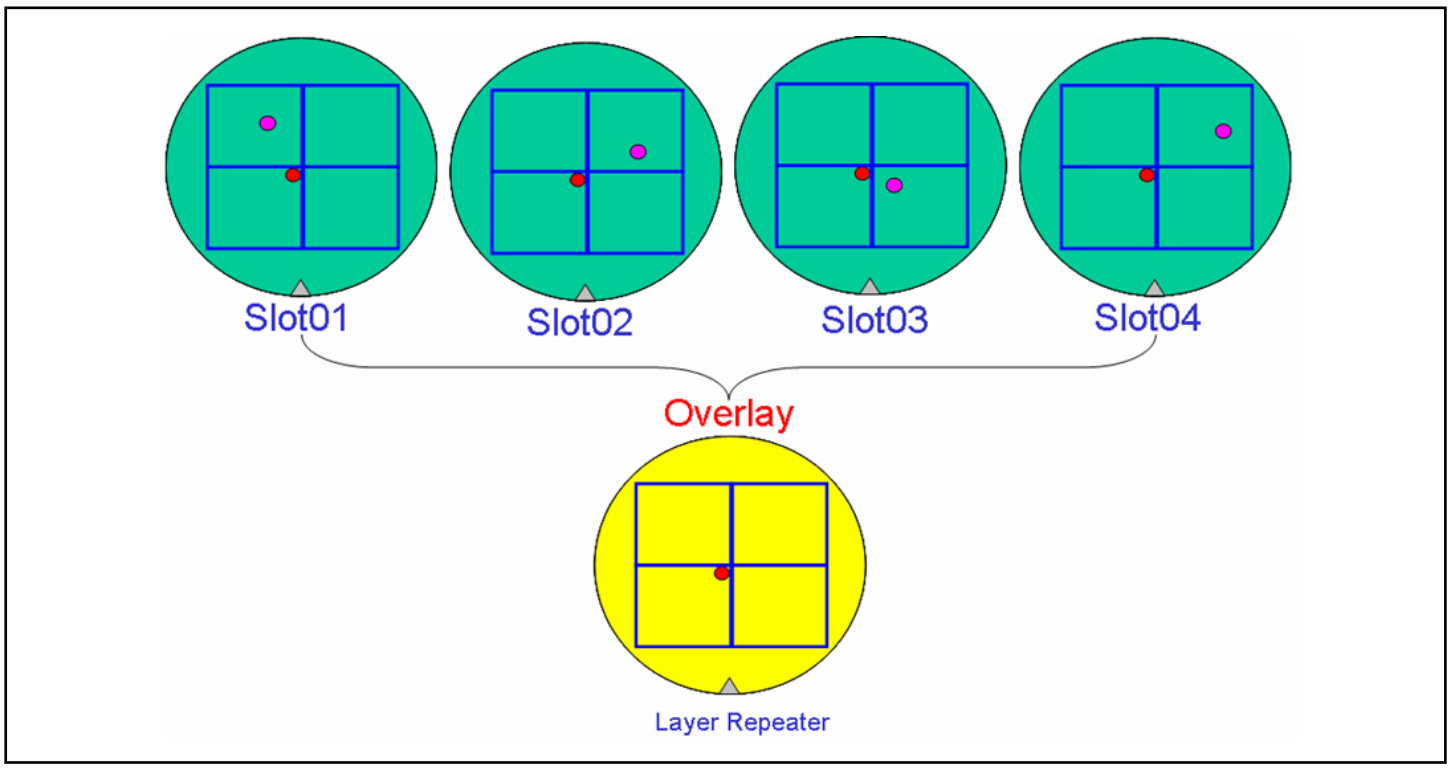

Figure 2 Overlaid wafer map with repeater

Layer repeater analysis

In this example, a recipe is used to overlay 4 wafer maps to determine if repeater defects are identified in the overlaid map; see Figure 3.

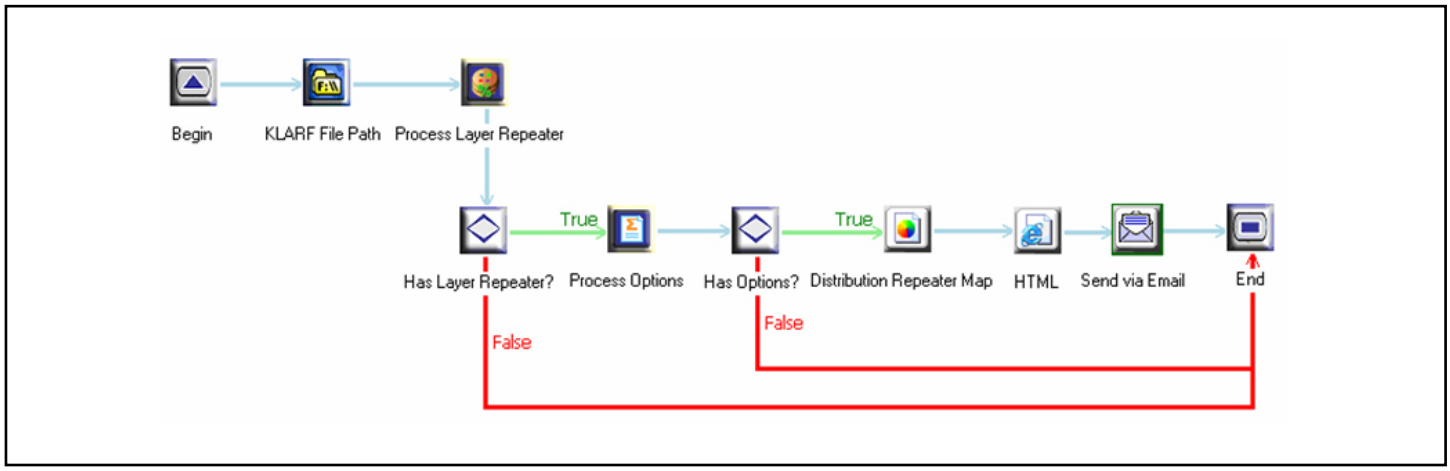

Figure 3 Layer repeater recipe

In this analysis, the layer repeater parameters are set as follows:

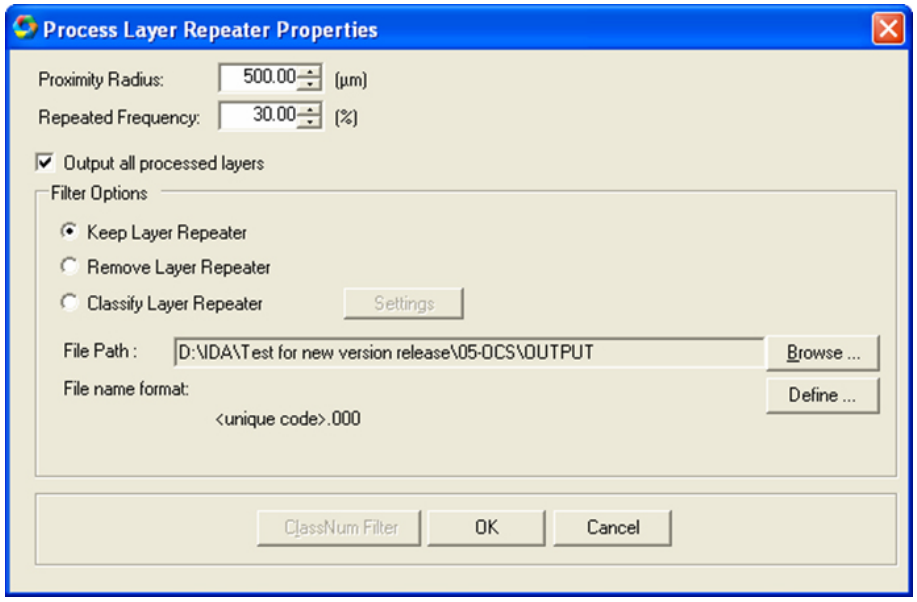

Figure 4 Layer repeater parameters

Example results

ILayer repeater was used to identify real root cause of manufacturing problems and set up a proper preventive maintenance procedure to prevent its recurrence. Figures 5 through 9 show the results of actual manufacturing problems that were detected by layer repeater analysis. The small wafer maps on the right side of each figure are a sample of the individual maps that were overlaid for the analysis. The large wafer map on the left side of each figure shows a map of the repeater locations. As the number of wafers containing the repeater increases, the die color becomes darker.

Layer repeaters were identified in the following manufacturing processes:

- Slurry residue at wafer edge (CMP) – Figure 5
- CMP overpolish – Figure 6
- Stepper chuck defocus – Figure 7
- Pattern deformity in PR (photoresist) etchback – Figure 8
- Scratch by process tool – Figure 9

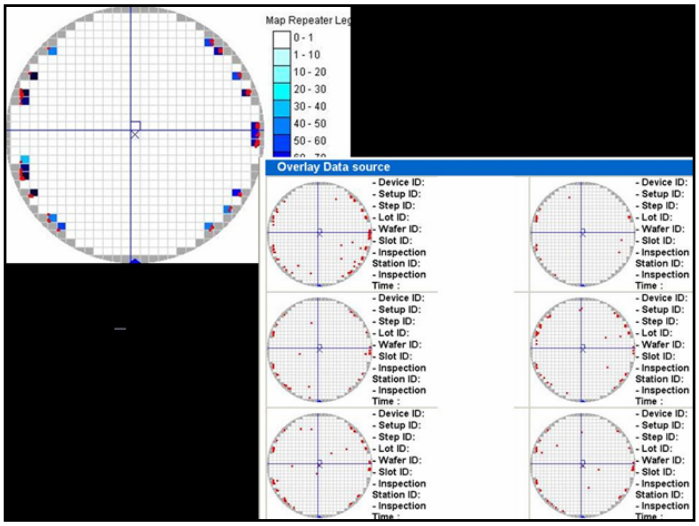

Figure 5 Slurry residue at wafer edge (CMP)

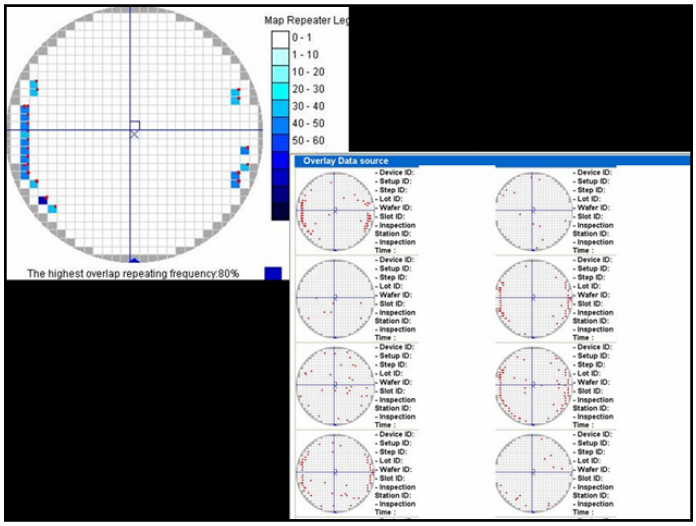

Figure 6 CMP Overpolish

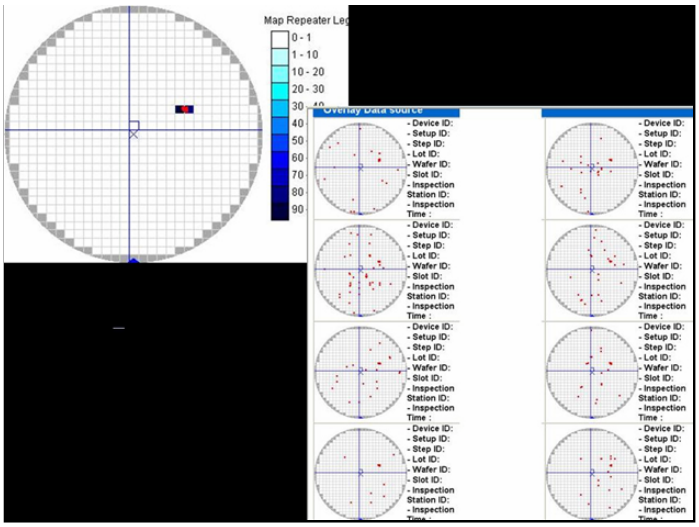

Figure 7 Chuck defocus from stepper

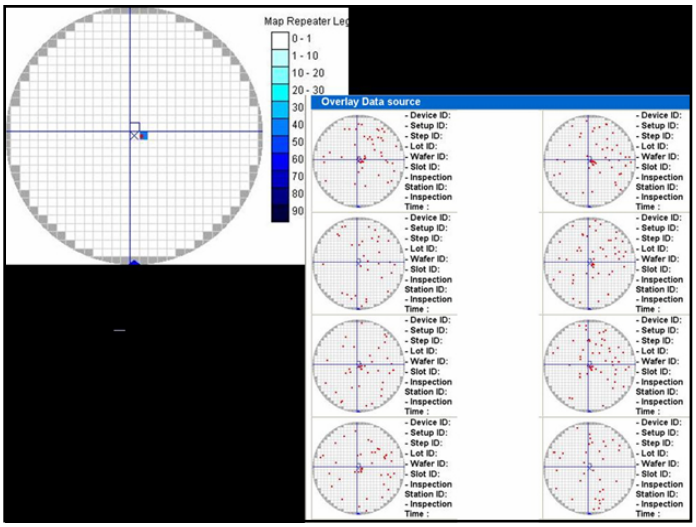

Figure 8 Pattern deform in PR (Photoresist) Etchback

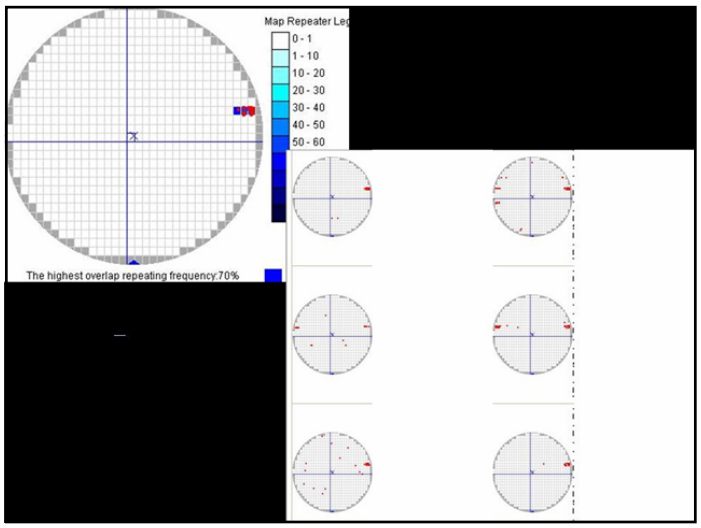

Figure 9 Scratch by process tool

Conclusion

This approach has the following advantages:

1. Only one recipe is required to analyze all *Device* and *Step.*
2. It's very simple to setup and monitor without training or using a pattern library.
3. Recipe is quite simple to maintain.
4. Very effective to monitor defect excursions affecting baseline yield